UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/912,683	07/24/2001	Austin H. Lesea	X-895 US	7141

24309 7590 02/09/2004

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	5

DATE MAILED: 02/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/912,683	LESEA, AUSTIN H.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 24 July 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date papers 2 and 4.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 are presented for examination.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on July 24, 2001 (paper 2) and the IDS submitted on October 28, 2002 (paper 4) have been considered by the examiner. Form 1449 has been signed and returned with this office action for each IDS.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the circuitry which is connected and then reprogrammed to achieve other applications (methods may be shown in flow chart form), and proper connections of circuitry must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

The drawings are objected to because descriptive labels other than numerical are needed for figure 1. See 37 CFR 1.84(o). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 3 and 5-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 3, the term "stresses" as applied to a clock signal in claim 3 is unclear.

As per claim 18, the phrase "or other stress or test pattern" is unclear.

Independent claims 5, 10, 14, and 17 are unclear with respect to "SERDES circuitry" and later uses of "SERDES" (without circuitry) having possible antecedent basis issues.

Independent claims 5, 10, 14, and 17 are also unclear with respect to "FPGA" and later uses of "array" or "logic array" having possible antecedent basis issues.'

Claims 5, 10, 14, and 17 are also unclear as to how the circuitry is operably connected in order to achieve the desired output.

Dependent claims 6-9,11-13, 15-16, and 18-20 inherit the 35 U.S.C. 112, second paragraph issues of the independent claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Kean et al. U.S. Patent No. 5,737,235.

As per claims 1-4 Kean et al. teach allowing the same pad to be used for both configuration and user interface, making partial dynamic reconfiguration convenient, and offers the user choices for controlling logic functions from within the FPGA and choices for interfacing with structures outside the FPGA. It also allows the FPGA chip to be loaded with configuration information either from parallel address and data pins or from a serial data pin. In an FPGA integrated circuit chip, a programmable switch is placed between the pins or pads of the chip and the internal circuitry of the chip. The internal circuitry includes logic which is accessed by a user during operation of the FPGA and configuration memory which controls the functions performed by the FPGA chip. The programmable switch adopts an initial state upon power-up to connect selected external pins to the configuration memory so that the configuration memory can be loaded. However, the configuration memory programs not only the internal circuitry accessed by the user but also the programmable switch itself. Thus as configuration proceeds, or after configuration is completed, the programmable switch can be reconfigured to connect signal lines of the FPGA user logic to lines for addressing or controlling the configuration memory which were initially loaded from external pins. A programmable switch which is initially configured to connect its related pad or pads to configuration control lines can later be configured to connect an

internally generated signal or signals to the line or lines and thus override any external signal which would have been connected to that line or lines. (Column 4 line 40 through column 5 line 40, figure 17)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 5, 8-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kean et al. U.S. Patent No. 5,737,235 in view of "Digital Systems Testing and Testable Design" Abramovici et al. (c) 1990 IEEE Press.

As per claims 5, 10, 14, 17 and 19, Kean et al. substantially teach the claimed system and method of allowing the same pad to be used for both configuration and user

interface, making partial dynamic reconfiguration convenient, and offers the user choices for controlling logic functions from within the FPGA and choices for interfacing with structures outside the FPGA. It also allows the FPGA chip to be loaded with configuration information either from parallel address and data pins or from a serial data pin. In an FPGA integrated circuit chip, a programmable switch is placed between the pins or pads of the chip and the internal circuitry of the chip. The internal circuitry includes logic, which is accessed by a user during operation of the FPGA and configuration memory, which controls the functions performed by the FPGA chip. The programmable switch adopts an initial state upon power-up to connect selected external pins to the configuration memory so that the configuration memory can be loaded. However, the configuration memory programs not only the internal circuitry accessed by the user but also the programmable switch itself. Thus as configuration proceeds, or after configuration is completed, the programmable switch can be reconfigured to connect signal lines of the FPGA user logic to lines for addressing or controlling the configuration memory which were initially loaded from external pins. A programmable switch which is initially configured to connect its related pad or pads to configuration control lines can later be configured to connect an internally generated signal or signals to the line or lines and thus override any external signal which would have been connected to that line or lines. (Column 4 line 40 through column 5 line 40, figure 17) Not explicitly disclosed is the self-testing of the circuit.

However in an analogous art, Abramovici et al. teach that programmable logic arrays can implement any Boolean function (page 593 paragraph 1) and also teach

circuits and methods of performing built in self-tests (BIST) of programmable logic arrays (14.4.2.2 page 605). Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the testing system of Abramovici et al. with the FPGA system of Kean et al. This would have been obvious as suggested by Abramovici et al. (Page 593 paragraph 1) as the book teaches an entire section of BIST for programmable gate arrays.

As per claims 8, 9, 12, and 13, Abramovici teaches using error detection methods in conjunction with BIST of programmable gate arrays in order to increase testability (page 600-607 14.4.1)

As per claims 11, and 18, Abramovici et al. teach using feedback shift registers to generate test functions. (Page 605 14.4.2.2).

As per claims 15, 16 and 19 Abramovici et al. teach getting test results from the programmable gate arrays (page 605 14.4.2.2).

Claims 6,7, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kean et al. U.S. Patent No. 5,737,235 and "Digital Systems Testing and Testable Design" Abramovici et al. (c) 1990 IEEE Press as applied to claim 5, and 8-19 above, and further in view of Frisch et al. U.S. Patent No. 6,295,315.

As per claims 6, 7, and 20 Kean et al. teach allowing the same pad to be used for both configuration and user interface, making partial dynamic reconfiguration convenient, and offers the user choices for controlling logic functions from within the FPGA and choices for interfacing with structures outside the FPGA. It also allows the FPGA chip to be loaded with configuration information either from parallel address and data pins or from a serial data pin. In an FPGA integrated circuit chip, a programmable switch is placed between the pins or pads of the chip and the internal circuitry of the chip. The internal circuitry includes logic, which is accessed by a user during operation of the FPGA and configuration memory, which controls the functions performed by the FPGA chip. The programmable switch adopts an initial state upon power-up to connect selected external pins to the configuration memory so that the configuration memory can be loaded. However, the configuration memory programs not only the internal circuitry accessed by the user but also the programmable switch itself. Thus as configuration proceeds, or after configuration is completed, the programmable switch can be reconfigured to connect signal lines of the FPGA user logic to lines for addressing or controlling the configuration memory which were initially loaded from external pins. A programmable switch which is initially configured to connect its related pad or pads to configuration control lines can later be configured to connect an internally generated signal or signals to the line or lines and thus override any external signal which would have been connected to that line or lines. (Column 4 line 40 through column 5 line 40, figure 17). Abramovici et al. teach that programmable logic arrays can implement any Boolean function (page 593 paragraph 1) and also teach performing built

in self-tests (BIST) of programmable logic arrays (14.4.2.2 page 605). Not explicitly disclosed is the method of testing for jitter.

However, in an analogous art, Frisch et al. a Jitter measurement system and process are described as being generally applicable to measuring jitter in periodic signals. In some implementations, however, the jitter measurement system process may be employed in connection with built-in self test (BIST) components of larger integrated circuits such as application specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), as well as integrated circuits that include or employ phase-locked loops. (Column 4 line65 through column 5 line 9) therefore as suggested by Frisch et al above it would have been obvious to a person having ordinary skill in the art at the time this invention was made to use the jitter testing methods of Frisch et al with the system of Abramovici et al. and Kean et al. as combined above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CB

Cynthia Britt
Examiner
Art Unit 2133

Gregory J. Lamarre for

Albert DeCady
Primary Examiner